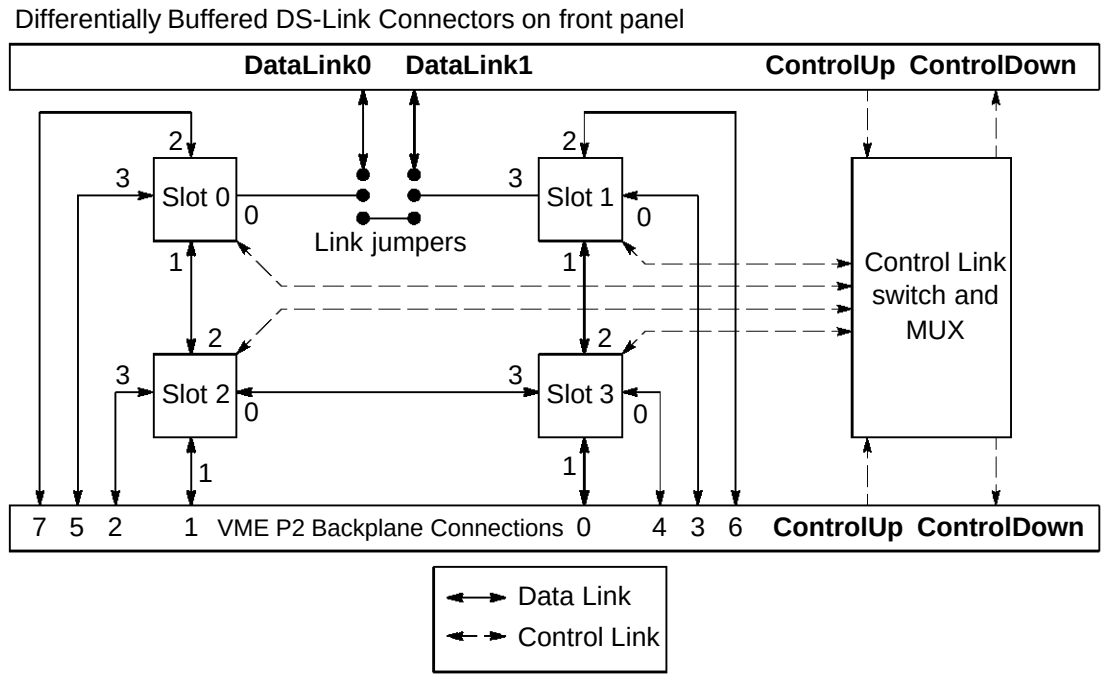
SGS-THOMSON MICROELECTRONICS

IMS B101

VME FORMAT HTRAM MOTHERBOARD



FEATURES

- Single slot-width, 6U VME format HTRAM motherboard
- 4, size 2, HTRAM slots to expand development systems for multiprocessor applications
- Fixed on-board DS data link connections make it easy to build pipelines, arrays and cubes of processors
- Differentially buffered front panel sockets for control and data links: compatible with INMOS development systems hardware
- Eight DS data links available via P2 backplane connector make it easy to use several boards to build larger systems
- Configurable control link pipeline allows full or part population with HTRAMs
- Compatible with INMOS development systems hardware and software

DESCRIPTION

The IMS B101 is designed for use as part of a development system for multiprocessors, parallel applications, or as a component of an HTRAM based OEM product.

It is a 6U VME format HTRAM motherboard, which can carry up to four, size 2 HTRAM supercomponents.

Connections to the control and data networks of the IMS B101 are available on the front panel – for connection to a host computer system during development work; or on the VME P2 connector for constructing larger systems from several IMS B101s or other compatible components

The combination of some fixed DS-Link connections on the motherboard and the backplane access will allow IMS T9000 systems of considerable complexity to be built without requiring external cables.

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1.1 IMS B101 specification

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The combination of some fixed DS-Link connections on the motherboard and the backplane access will allow IMS T9000 systems of considerable complexity to be built without requiring external cables.

Although totally compatible with standard VME backplanes and enclosures, the IMS B101 requires only appropriate power connections, and does not participate in any VME bus protocols or transactions.

The physical layout of the IMS B101 is shown in figure 1.1. There are eight physical HTRAM sockets on board, configured as four logical size 2 slots.

Up to four size 2 HTRAMs, two size 4 HTRAMs, or a mixture of size 2 and size 4 HTRAMs can be installed on the IMS B101. (Odd sized HTRAMs cannot be installed on an IMS B101).

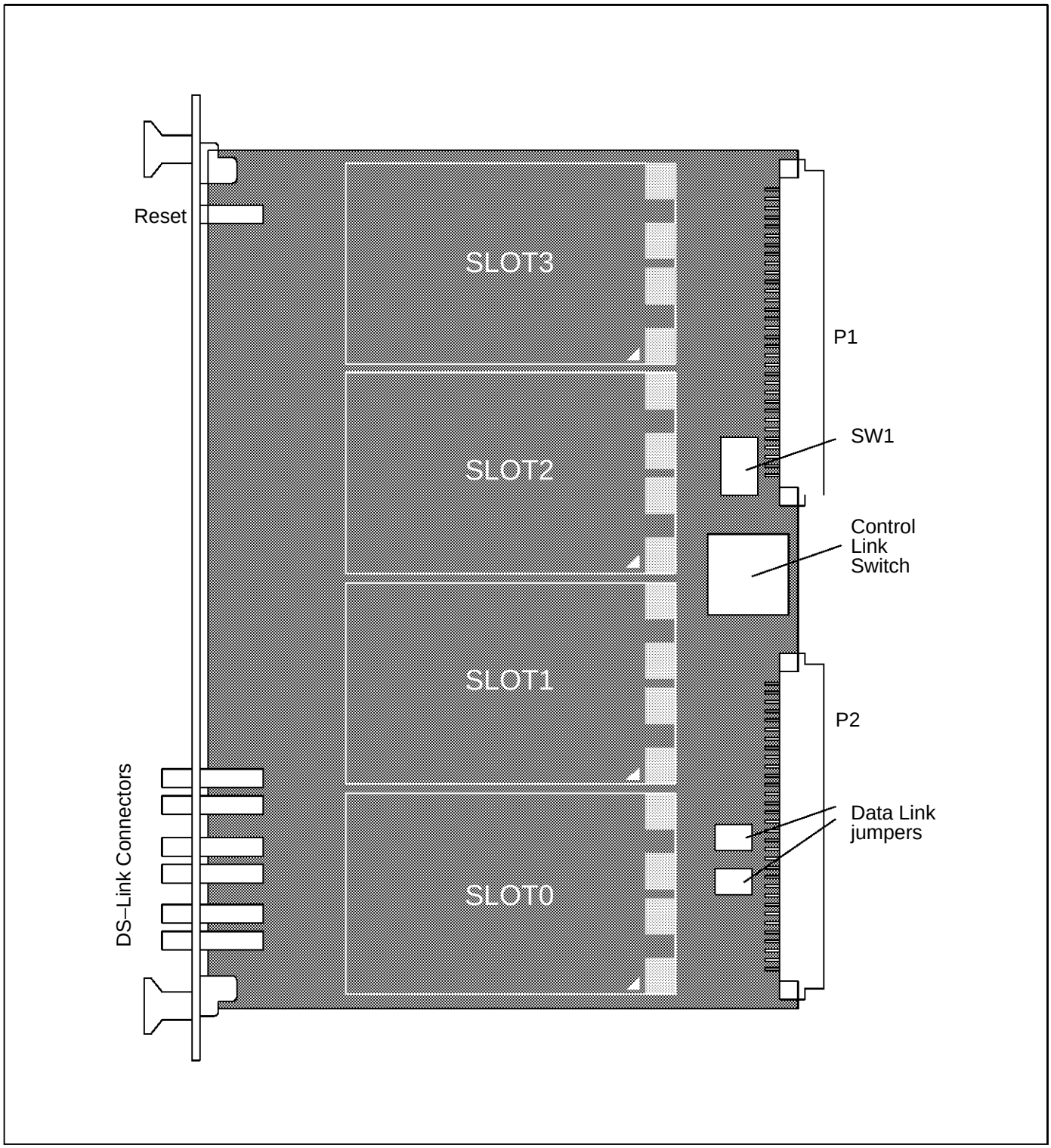

Figure 1.1 IMS B101 layout

1.1.1 Control link network

After a system of HTRAMs is reset, it must be *configured* and then loaded with an application program. This is done by means of a network of *control links*, separate from the data link network.

Each HTRAM has a **ControlUp** link connection, and a **ControlDown** link connection. In a system, these are commonly connected as a 'daisy-chain' or pipeline: **ControlDown** of one HTRAM to **ControlUp** of the next, with **ControlUp** of the first HTRAM connected to the host system or board which resets the network and loads the software. (**ControlDown** of the last HTRAM is left unconnected).

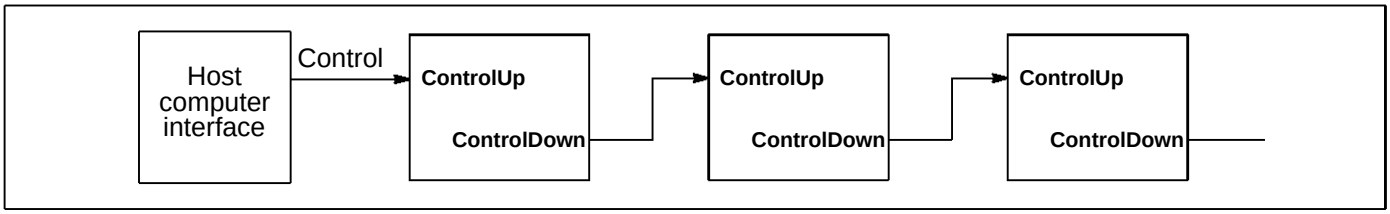

Figure 1.2 Pipeline of control links

The IMS B101 implements a pipelined connection of control links through up to four HTRAMs. It provides a choice of connections to **ControlUp** of the first HTRAM, and to **ControlDown** of the last HTRAM, either through connectors on the front panel or through the P2 connector to a system backplane. This allows the user to build systems using multiple IMS B101s easily. For flexibility, there is a control link switch which allows the IMS B101 to be used with only some of the HTRAM slots populated, while maintaining the control link pipeline through the board. This switch also provides a choice of off-board connection through the front panel or P2 connector.

If there are one or more unpopulated slots, the **ControlDown** from the last occupied slot should be connected directly to **ControlDown** on the front or rear panel using the control link switch.

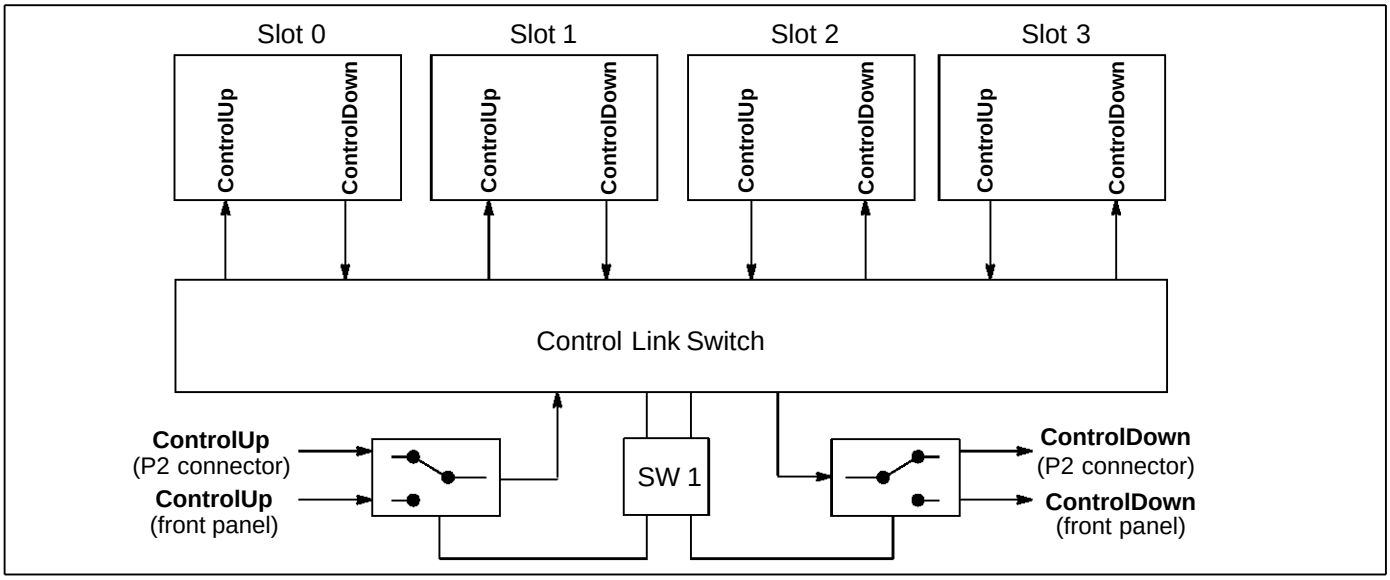

Figure 1.3

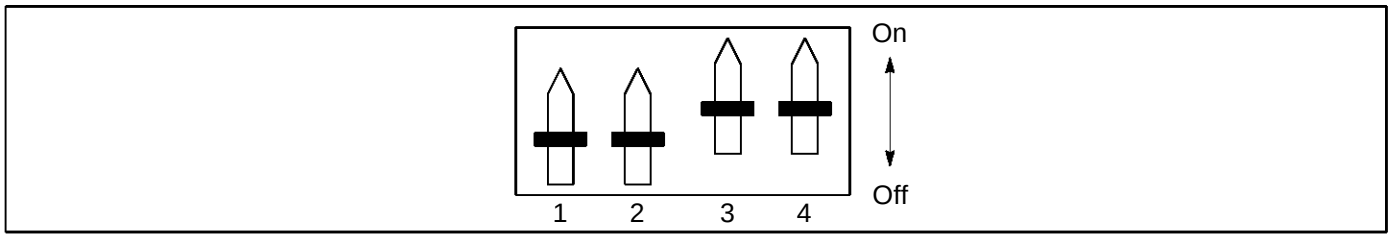

Figure 1.4 Switch SW1

SW1:1	SW1:2	Source for External Control Link Down
ON	ON	SLOT 0 **ControlDown**
ON	OFF	SLOT 1 **ControlDown**
OFF	ON	SLOT 2 **ControlDown**
OFF	OFF	SLOT 3 **ControlDown**

SW1:3	Source for IMS B101 Control Link Up
ON	**ControlUp** from VME_P2 backplane
OFF	**ControlUp** from DS-Link connectors on front panel

SW1:4	Destination of IMS B101 Control Link Down
ON	**ControlDown** to VME_P2 backplane
OFF	**ControlDown** to DS-Link connectors on front panel

Table 1.1 SW1 configuration settings

HTRAMs must always be installed beginning in slot 0 and continuing in order through to slot 3. (This is to maintain the connection of the control link pipeline through the IMS B101). The settings of SW1, depend on which is the last slot on the board occupied by an HTRAM.

Example configuration	Last slot occupied	SW1:1	SW1:2
1 x size 4	1	ON	OFF
1 x size 2	0	ON	ON
1 x size 4 + 1 x size 2	2	OFF	ON
2 x size 2	1	ON	OFF
Many other configurations are possible			

Note:
Due to the switching arrangement of the control links on the IMS B101, it is not possible to run the T9000 control network reliably at speeds of greater than 20Mbit/s. This restriction should be reflected in the Network Description Language files for the system.

1.1.2 Data link network

The data link arrangement is shown in figure 1.5. Some fixed data link connections are provided between HTRAM slots on the motherboard with jumpers (figure 1.6) allowing optional connections to front panel connectors. The remaining data links from the HTRAM slots are taken, in unbuffered form, to the P2 backplane connector. Connections to other similar motherboards through a special backplane allow systems of considerable size to be constructed without resort to front panel patch cables. The arrangement of data link connections shown in figure 1.5 makes it easy to construct systems of HTRAMs connected as simple pipelines, arrays, or cubes.

However, special consideration should be taken when making use of DS-Links on the P2 connector since they operate at very high frequencies. It is not recommended that any unshielded method of link distribution be used, such as unshielded ribbon cable, or any similar media.

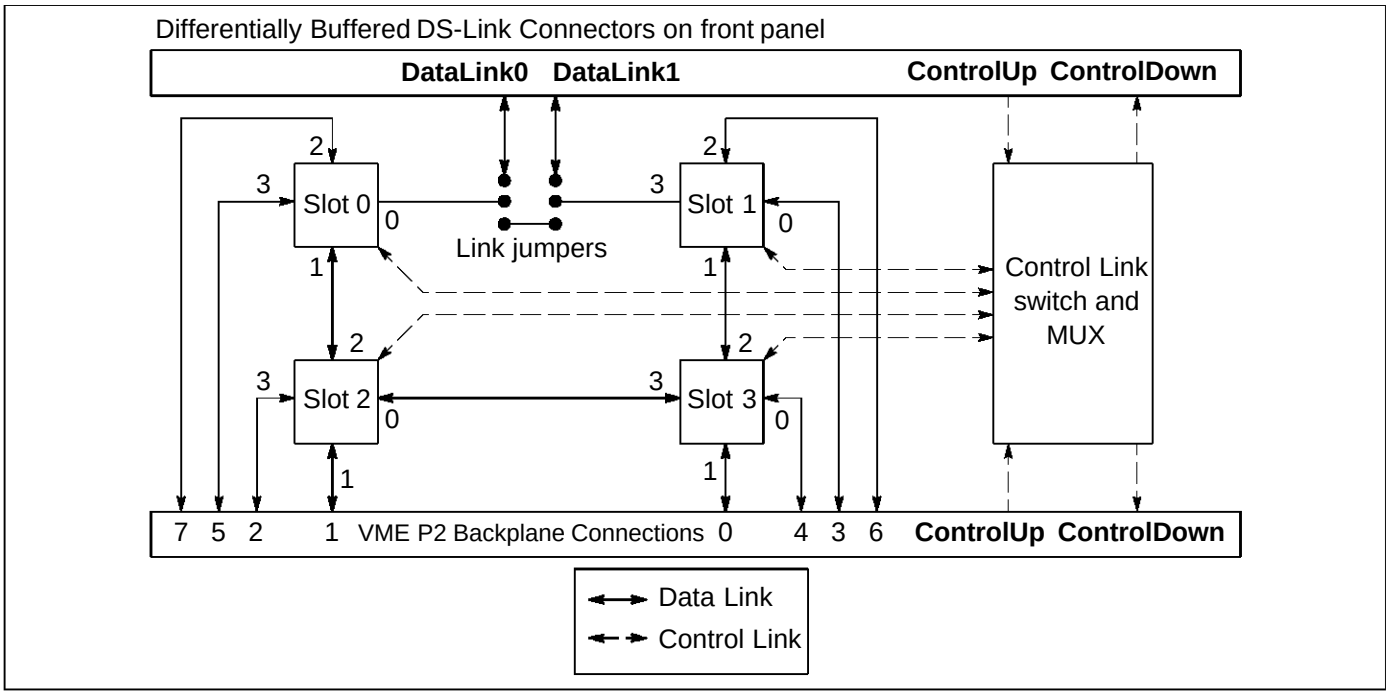

Figure 1.5 Data link connections

Two data links from slot 0 and slot 1 can optionally be accessed through connectors on the front panel, for connection to an interface in a host computer system for the loading of code and communication of data. Alternatively these data links complete the square of connections between the HTRAMs. The choice of these data link connections is made by setting jumpers JP1 – JP8 appropriately, as shown in figure 1.6.

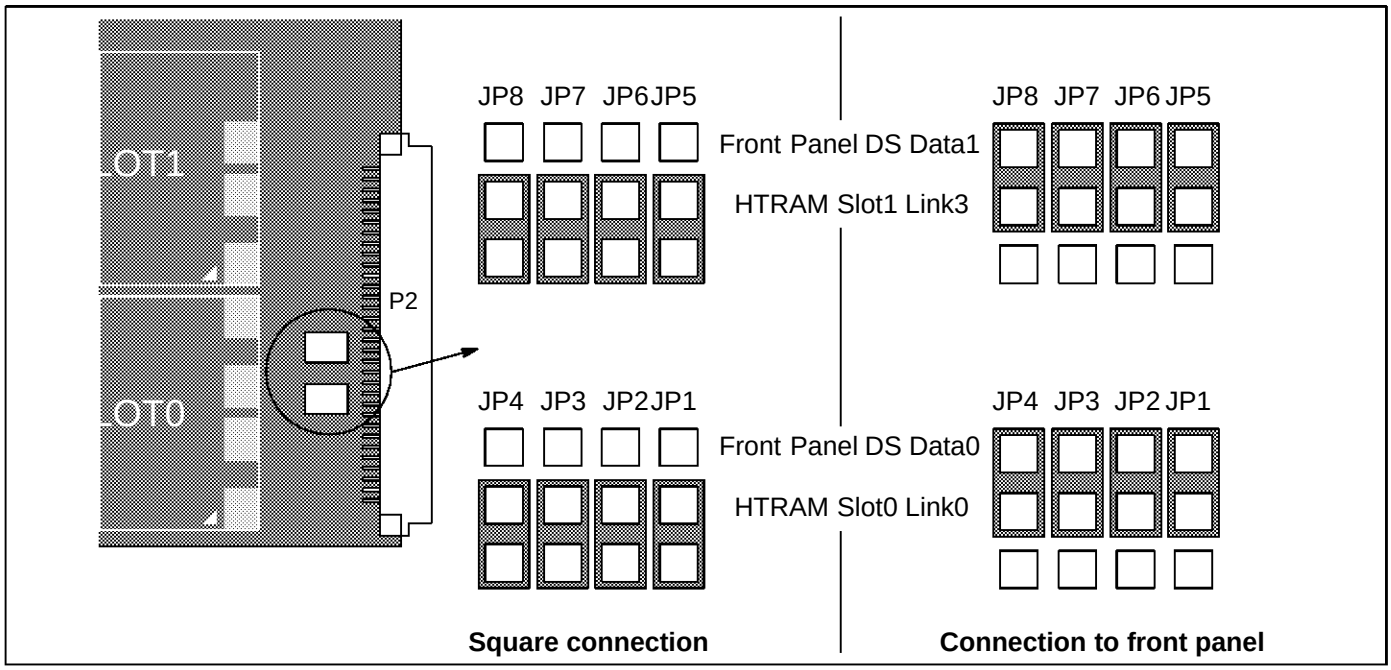

Figure 1.6 Jumper settings

1.1.3 Front panel connections

Control links, data links and reset connections are all available from connectors on the front panel. This allows the user to connect the IMS B101 to an interface in a host computer for loading code and data and also to connect to other boards when building larger systems.

Two DS data links and each end of the DS control link pipeline are differentially buffered and can be accessed via DS-Link modular connectors brought to the front panel. An additional pair of connectors are provided for a hardware reset signal to be accessed via a similar differential buffering scheme. The front panel layout is shown in figure 1.7.

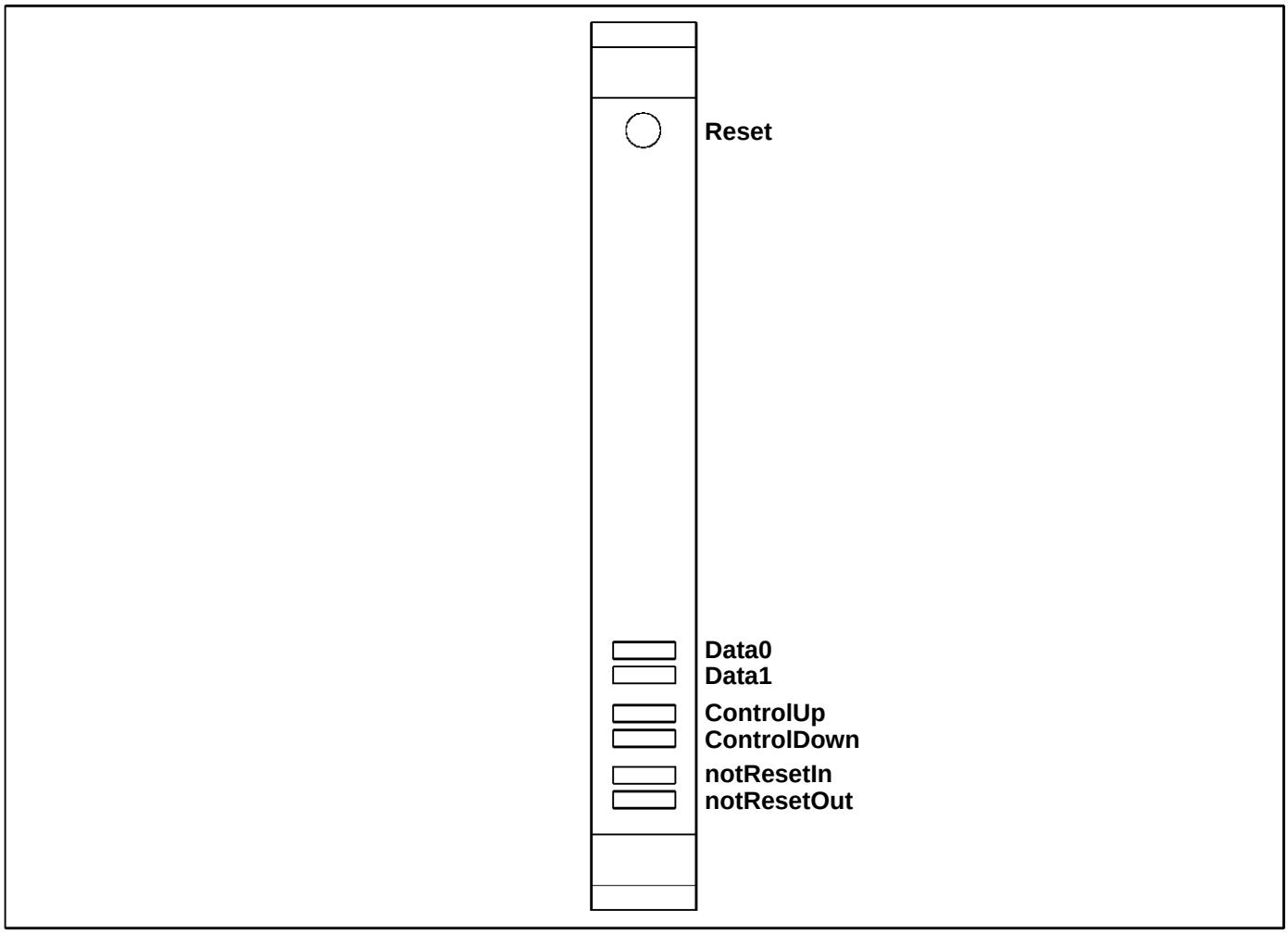

Figure 1.7 IMS B101 front panel

Full details on the use of external DS-Link connections between separate pieces of equipment and the host reset connection standard are defined in [6].

1.1.4 Connecting the IMS B101 to a host interface

The IMS B101 can be connected to a host computer interface, or network interface board, and used as part of a software development system.

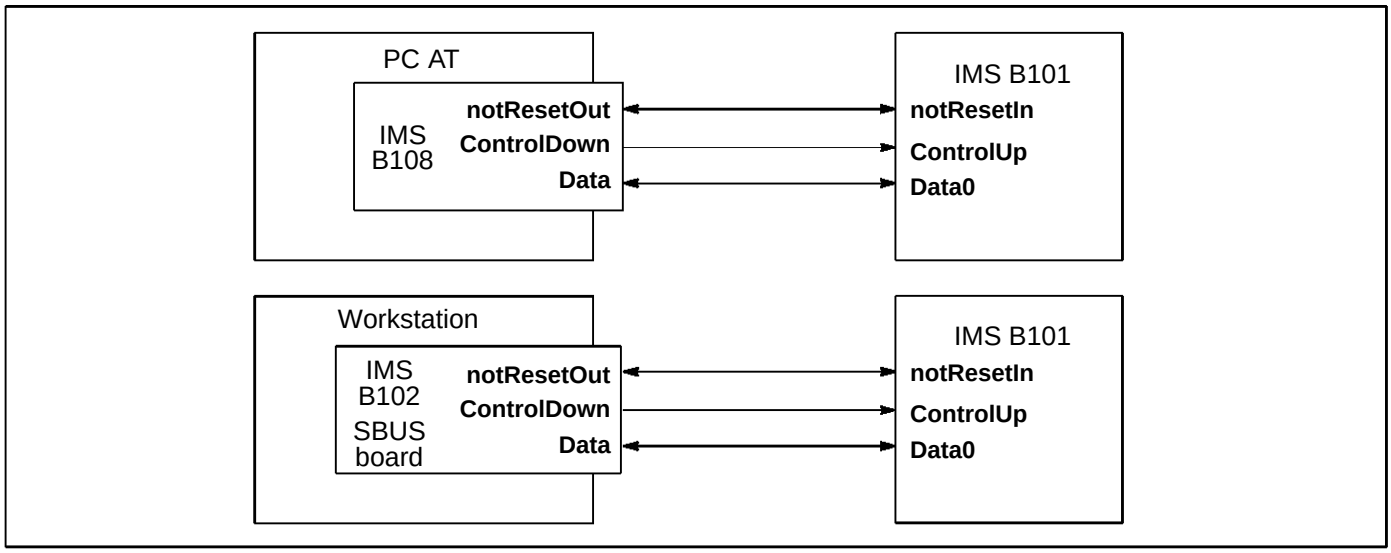

Figure 1.8 Connection to a host interface

When connecting to a host interface board, such as an SBUS or PC add-in board, this is most easily done using the connectors on the IMS B101 front panel (rather than the P2 connector). The IMS B101 must be configured to use the front panel connections, (refer to figure 1.6 and table 1.1). Three simple connections should be made as follows:

Host board	IMS B101
notResetOut	notResetIn
ControlDown	ControlUp
Data	Data0

Table 1.2

This allows the host board to reset and control the IMS B101 so that development system software running on the host computer can load, run and debug programs on HTRAMs on the IMS B101.

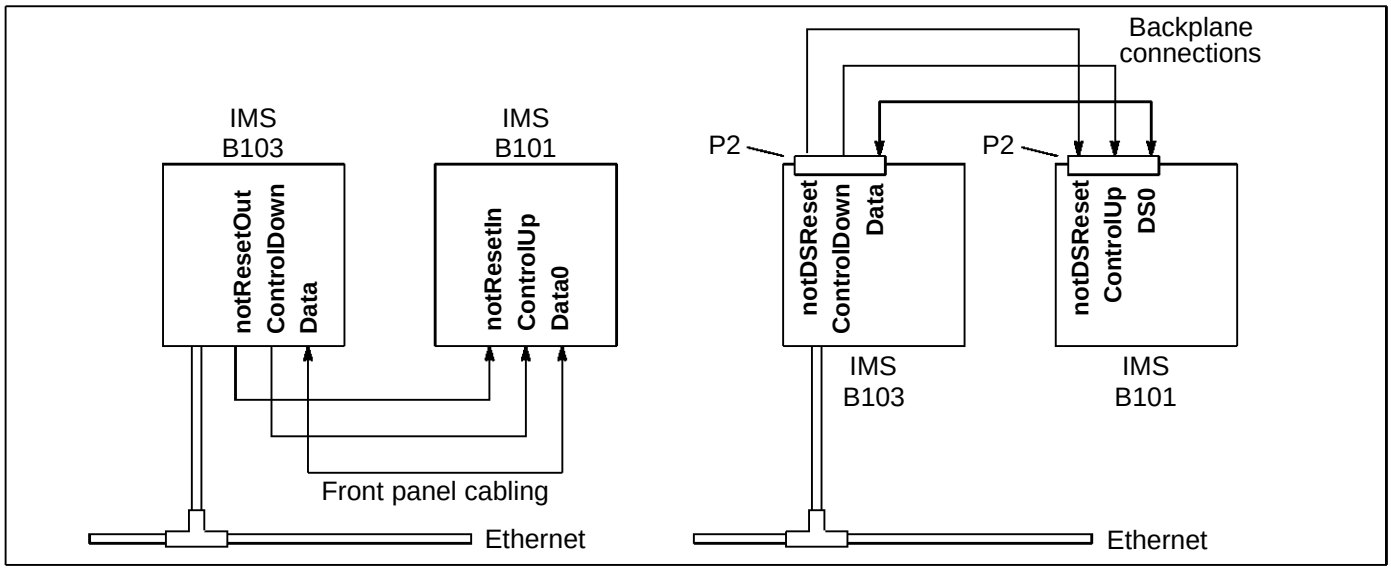

Figure 1.9 Connections to networks of interface boards

When connecting to a network interface board such as the IMS B103, the user has a choice of either: making the reset, control, and data link connections through the front panel connectors, or through the P2 connector of both boards (perhaps via a special backplane). In either case, the user must configure both boards to use the required connectors.

1.1.5 Building larger systems

Several IMS B101s can be connected together to build larger HTRAM systems:

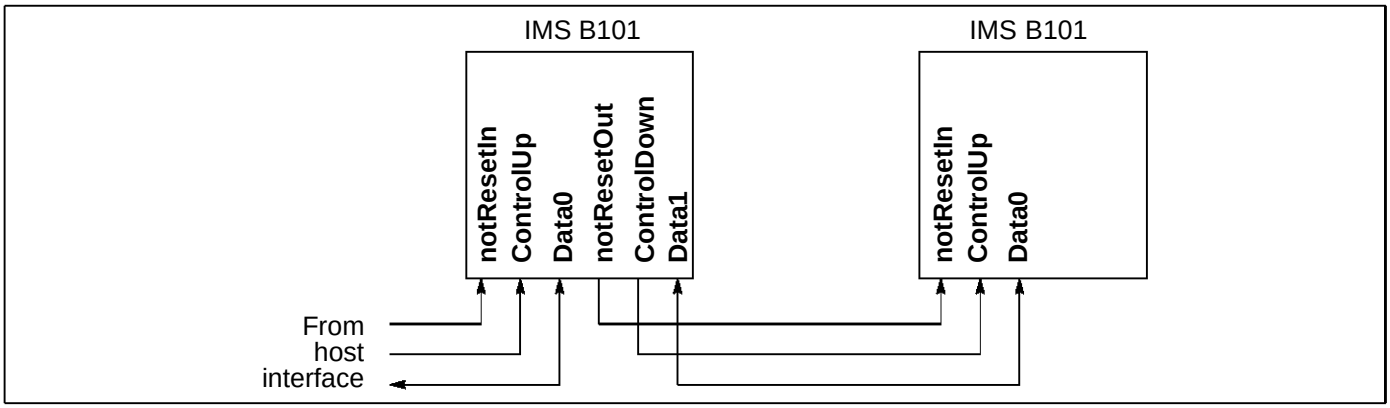

Figure 1.10

Connections between boards can be made either between the front panel connectors or through the P2 connectors. The boards must be configured to use the desired set of connections.

Simple systems using multiple B101s can be built using only front panel connections for data links. However, using the link connections on P2 allows more highly-connected networks to be built since more connections are available.

If connections are to be made through the P2 connectors, it is recommended that a controlled impedance (100Ω) backplane is used as the link signals are very high frequency, and therefore not suitable for connection with wire-wrap or similar techniques.

1.1.6 Installing HTRAMs

HTRAMs are installed as follows:

- Find the desired slot on the HTRAM motherboard
- Align the yellow triangle marked on the HTRAM PCB with the corresponding symbol on the HTRAM motherboard
- Insert the pins on the underside of the HTRAM into the sockets on the motherboard, and press home. (Take care to ensure that this is done with the correct alignment)
- Check that the fixing holes in the HTRAM are correctly aligned with the threaded posts on the motherboard
- Use M3 bolts, if required, to secure the HTRAM to the motherboard.

1.1.7 Example software description of 4 HTRAM network on an IMS B101 (NDL file)

```
#INCLUDE ”stdndl.inc”

CONTROLPORT host :
HOST IS host[data] :
CONTROL IS host[control] :

ARC HostLink :
[3]NODE Node :
NODE RootNode :
NETWORK
  DO
    -- set default attributes
    SET DEFAULT (link.speed.multiply  := 10)
    SET DEFAULT (link.speed.divide    := [1])
    SET DEFAULT (control.speed.divide := [8])

    -- set device attributes for root node
    SET RootNode (type             := ”T9000”)
    SET RootNode (root             := TRUE)
    SET RootNode (local.rom        := FALSE)
    SET RootNode (pmi.config.inrom := FALSE)
    SET RootNode (cachesize        := 16)
    SET RootNode (memconfig        := RamMemoryFile)
    SET RootNode (memory           := RamMemoryRegions)

    -- set device attributes for rest of network
    DO i = 0 FOR SIZE Node
      DO
        SET Node[i] (type             := ”T9000”)
        SET Node[i] (local.rom        := FALSE)
        SET Node[i] (pmi.config.inrom := FALSE)
        SET Node[i] (cachesize        := 0)
        SET Node[i] (memconfig        := RamMemoryFile)
        SET Node[i] (memory           := RamMemoryRegions)

    -- form daisychain control network
    CONNECT RootNode[control.up] TO CONTROL

    CONNECT RootNode[control.down] TO Node[0][control.up]
    DO i = 0 FOR (SIZE Node) – 1
      CONNECT Node[i][control.down] TO Node[i + 1][control.up]

    -- connect onboard data network (with initial front panel link)
    CONNECT RootNode[link][0] TO HOST WITH HostLink
    CONNECT RootNode[link][1] TO Node[1][link][2]
    CONNECT Node[0][link][1] TO Node[2][link][2]
    CONNECT Node[1][link][0] TO Node[2][link][3]
:
```

1.1.8 VMEbus

The IMS B101 does not have a VMEbus interface. Only VME ***SYSRESET** is used by the board. 'Jumpering' of the **IACK** and **BusGrant** VMEbus signals is provided. No other connections apart from power are made to the VMEbus backplane.

Pin	Row C	Row B	Row A
1			
2			
3			
4		***BG0IN**	
5		***BG0OUT**	
6		***BG1IN**	
7		***BG1OUT**	
8		***BG2IN**	
9	**GND**	***BG2OUT**	**GND**
10		***BG3IN**	
11		***BG3OUT**	**GND**
12	***SYSRESET**		
13			
14			
15			**GND**
16			
17			**GND**
18			
19			**GND**
20		**GND**	
21			**IACKIN***
22			**IACKOUT***
23		**GND**	
24			
25			
26			
27			
28			
29			
30			
31	**+12V**		**–12V**
32	**+5V**	**+5V**	**+5V**

Note: All remaining pins are not connected

Figure 1.11 P1 connections

		C	B	A	
DS3	1	DIN	VCC	DOUT	DS4
	2	GND	GND	GND	
	3	SIN		SOUT	
	4	SOUT		SIN	
	5	GND		GND	
	6	DOUT		DIN	
DS2	7	DIN		DOUT	DS5
	8	GND		GND	
	9	SIN		SOUT	
	10	SOUT		SIN	
	11	GND		GND	
	12	DOUT	GND	DIN	
DS1	13	DIN	VCC	DOUT	DS6
	14	GND		GND	
	15	SIN		SOUT	
	16	SOUT		SIN	
	17	GND		GND	
	18	DOUT		DIN	
DS0	19	DIN		DOUT	DS7
	20	GND		GND	
	21	SIN		SOUT	
	22	SOUT	GND	SIN	
	23	GND		GND	
	24	DOUT		DIN	
ControlDown	25	DIN		DOUT	ControlUp
	26	SIN		SOUT	
	27	GND		GND	
	28	SOUT		SIN	
	29	DOUT		DIN	
	30	notDSRESET		RESERVED	
	31	VCC	GND	VCC	
	32	VCC	VCC	VCC	

Figure 1.12 P2 connector pinout

1.1.9 Reset

The IMS B101 supports several sources of reset for itself and for any HTRAMs mounted in its respective slot. The reset sources are:

- Power-on reset
- Front panel reset (from button)
- VME ***SYSRESET** (from backplane P1)
- **notDSRESET** (from backplane P2)
- Front panel **ResetIn** connector

notDSRESET can be used in conjunction with a special backplane to supply or receive reset services when used in a multiple board T9000 system environment. The function of **DSRESET** is two fold: either to supply **notDSRESET** to all T9000 boards connected on the special J2 backplane or to receive a reset from any other card that has asserted **notDSRESET** on the backplane.

In addition to the above the IMS B101 has connectors for external **notResetIn** and **notResetOut**, giving a host the ability to reset the IMS B101. This or any other reset, (with the exception of ***SYSRESET**), performed upon the IMS B101 is propagated to **notResetOut**, allowing several IMS B101s to be reset from a single host. Further details on the **notResetIn** and **notResetOut** connections can be found in [6].

1.1.10 Power

The IMS B101 only requires a 5.0 Volt power supply, obtained through the VME P1 and P2 backplane connectors. The IMS B101 does not require 3.3 Volts to operate and does not supply 3.3 V to any of the HTRAM slots.

When plugged into a standard VME J1/J2 backplane the maximum allowable power dissipation of the IMS B101 at 60°C is 36W from the 5V power supply. This may limit the number of HTRAMs which can be fitted. However, additional power connections have been allocated on the VME P2 user defined pins and, when these are used in conjunction with a customised VME P2 backplane the maximum allowable power dissipation is increased to 60W – allowing the IMS B101 to be fully populated with HTRAMs.

1.1.11 Mechanical details

The IMS B101 is designed in accordance with the VMEbus standard [4]. The overall size of the board is 160mm by 233.35mm with a board thickness of 1.6mm. The supplied front panel width is 4HP, compatible with a board-to-board pitch in a card cage of 0.8''. Use of the IMS B101 with HTRAMs of height classes A and B results in an assembly that meets the VMEbus specification for a single width board. Note the front panel is required when operating the IMS B101 in a card cage, both for mechanical rigidity, to maintain correct air flow for cooling, and provide EMC shielding.

1.1.12 Cooling requirements

Adequate forced air cooling must be provided to ensure that components and HTRAMS are kept within their operating temperature. Failure to do so may affect the reliability of the motherboard and associated HTRAMS. Air flow should run parallel to the board surface and parallel to the front panel.

The cooling airflow requirements for the IMS B101 itself are defined in table 1.3. The datasheets for individual HTRAMs should be consulted to determine the system cooling requirements.

1.1.13 Operating Ranges

Functionality is not guaranteed outside the Operating Ranges. Operation beyond the Operating Ranges is not recommended and may affect device reliability.

Parameter	Min.	Typ.	Max.	Unit	Notes
Operating temperature	0		50	°C	
Airflow	0	2		m/s	1
+5V DC	4.875		5.25	V	
Power consumption (+5V DC)			4	W	2

1 It should be noted that adequate cooling airflow must be provided to maintain any fitted HTRAMs within their rated operating temperature.

2 Value shown is with **no** HTRAMs fitted.

Table 1.3 Operating Ranges

1.1.14 Absolute maximum ratings

Functionality at or above these limits is not implied. Stresses beyond the Absolute Maximum Ratings may cause permanent damage.

Parameter	Min.	Max.	Unit
Storage temperature	0	70	°C
Supply Voltage	0	7.0	V

Table 1.4 Absolute Maximum Ratings

1.2 Ordering information

Description	Order Number
VME format HTRAM motherboard	IMS B101-1

Table 1.5 Ordering information

The board is supplied with a copy of this datasheet. No cables or connectors are included, but these are available separately.

1.3 Field Support

INMOS products are supported worldwide through SGS-THOMSON Sales Offices and authorized distributors.

1.4 References

1 *T9000 Transputer Hardware Reference Manual,* INMOS Ltd 1993

2 *HTRAM specification*, INMOS Ltd 1994

3 *T9000 Brochure,* INMOS Ltd 1993

4 *IEEE Standard for a Versatile Backplane Bus: VMEbus*, IEEE 1987

5 *The Transputer Development and i***q** *systems Databook* INMOS Ltd (72-TRN-219-01)

6 *DS-Link, Connector Standards and Cabling*, INMOS Ltd 1994 (42–1634–00)